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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte YOSUKE MIZUTANI

Appeal 2011-005259
Application 12/000,629
Technology Center 2800

Before HUBERT C. LORIN, KAREN M. HASTINGS, and GEORGE C. BEST, *Administrative Patent Judges*.

BEST, *Administrative Patent Judge*.

DECISION ON APPEAL

On February 18, 2010, the Examiner finally rejected claims 1 and 4 of Application 12/000,629 under 35 U.S.C. § 103(a) as obvious. Appellant[1] seeks reversal of this rejection pursuant to 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

For the reasons set forth below, we AFFIRM.

BACKGROUND

The '629 application describes a semiconductor integrated circuit package comprised of a plurality of chips. Claims 1 and 4 are the only claims in the '629 application. Claim 1 is reproduced below:

> 1. A semiconductor integrated circuit in which a plurality of semiconductor chips are mounted in a single package, the circuit comprising:
>
> a cutoff circuit that stops the supply of power voltage from one of the semiconductor chips to another of the semiconductor chips,
>
> the plurality of semiconductor chips include a first semiconductor chip in which a logic circuit is formed, and a second semiconductor chip in which a semiconductor memory is formed,
>
> the cutoff circuit is provided within the first semiconductor chip, and
>
> the cutoff circuit is a switch element composed of an MOS transistor, and the switch element cuts off the supply of power voltage from the first semiconductor chip to the second semiconductor chip in a standby mode in accordance with a

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[1] Sanyo Electric Co. and Sanyo Semiconductor Co. are identified as the real parties in interest. (App. Br. 1.)

control signal from a power control circuit provided to the first semiconductor chip.

(App. Br. Claims App'x. A-1.)

REJECTIONS

On appeal, the Examiner maintains the following rejection:

Claims 1 and 4 are rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Tsuda[2] and Yamaoka.[3] (Ans. 5.)

DISCUSSION

Appellant argues that the Examiner erred in interpreting Yamaoka and that the rejection should be reversed because of this error.[4] (App. Br. 8.)

The Examiner found that Tsuda describes a semiconductor package comprising multiple chips in a single package. (Ans. 5.) Tsuda's semiconductor package includes a mother chip and a stack chip. (*Id.*) The mother chip includes logic circuitry, and the stack chip includes a semiconductor memory. (*Id.*) Yamaoka describes a semiconductor memory chip that includes a power cutoff circuit that is located outside of the memory circuit portion of the chip. (*Id.* at 6.)

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[2] U.S. Patent Application Publication No. 2002/0033526 A1, published March 21, 2002.

[3] U.S. Patent Application Publication No. 2003/0079705 A1, published April 24, 2003.

[4] Appellant argues for the reversal of the rejection of both claim 1 and claim 4, but presents arguments focused on claim 1's limitations. (App. Br. 8-10.) With respect to claim 4, Appellant merely asserts that claim 4 "recites similar features [to those recited in claim 1], each of which is not taught by the prior art." (*Id.* at 9.) Our discussion therefore focuses on claim 1 but applies to claim 4 with equal force.

The Examiner relied upon Yamaoka as describing or suggesting the following elements of the claims:

- a cutoff circuit provided within the first semiconductor chip,
- the cutoff circuit being a switch element composed of an MOS transistor,
- the switch element cutting off/stopping the supply of power voltage from the first semiconductor chip to the second semiconductor chip in a standby mode in accordance with a control signal from a power control circuit provided to the first semiconductor chip.

(*Id.* at 5.)

Appellant argues that the combination of Tsuda and Yamaoka does not create a prima facie case of obviousness because Yamaoka describes the cutoff circuit as being located on the memory chip, while claim 1 requires that the cutoff circuit be located on the mother chip. (App. Br. 9-10.)

The Examiner responds that a person of ordinary skill in the art would have been motivated to move the cutoff circuit from the stacked memory chip to the mother chip to reduce the number of connections that must be made between the mother chip and the stack chip. (Ans. 9-10.)

On this record, we do not find fault with the Examiner's conclusion. The Examiner has identified the differences between the prior art and the claimed invention as required by *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966), and has articulated reasoning supported by a sufficient rational underpinning to support the legal conclusion of obviousness, *see In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). The Examiner, therefore, has met the burden of establishing the prima facie obviousness of the claimed invention.

Appellant does not point us to any objective evidence of non-obviousness. Thus, we affirm the Examiner's rejection of claims 1 and 4 of the '629 application.

CONCLUSION

The Examiner correctly concluded that claims 1 and 4 of the '629 application would have been obvious to a person of ordinary skill in the art at the time of the invention in view of the combination of Tsuda and Yamaoka.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

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